



2.7W Filterless Class D Stereo Audio Amplifier

General Description

The MD2012 is a high efficiency, 2.7W/channel stereo class-D audio power amplifier. A low noise, filterless PWM architecture eliminates the output filter.

Operating from a single 5V supply, MD2012 is capable of delivering 2.7W channel of continuous output power to a 4Ω load with 10% THD+N.

The MD2012 features independent shutdown controls for each channel. The gain can be selected to 6, 12, 18, or 24 dB utilizing the G0 and G1 gain select pins. High PSRR and differential architecture provide increased immunity to noise and RF rectification.

The MD2012 is available in space-saving WCSP and TQFN packages, is an idea choice for mobile phones and other portable communication devices.

The MD2012 is available in a 4mm*4mm *0.75mm 20 pin QFN,TSSOP_20L package.

Features

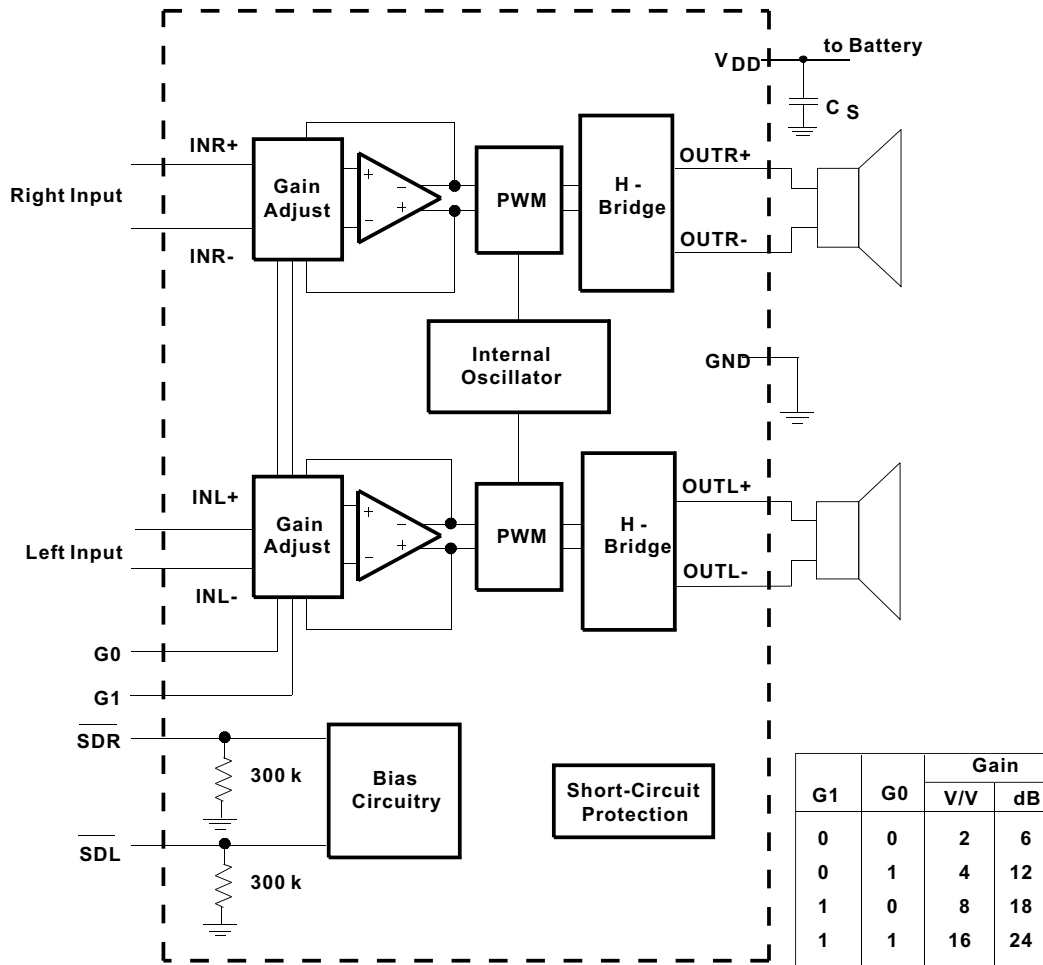
- Po at 10% THD+N, VDD = 5V
 $RL = 8\Omega$ 1.5W(type)
 $RL = 4\Omega$ 2.7W(type)
- Po at 10% THD+N, VDD = 3.6V
 $RL = 8\Omega$ 0.75W(type)
- 2.5-5.5V operation
- Unique Modulation Scheme Reduces EMI Emission
- Independent Shutdown Control for Each Channel
- Selectable Gain of 6,12,18 and 24dB
- Internal Pulldown Resistor On Shutdown Pins
- High PSRR :74dB at 217Hz
- Fast 10ms Startup Time
- Thermal and over current Protections
- RoHS compliant and 100% lead(Pb)-free

Applications

- Mobile Phones
- PDA,GPS
- Portable Electronic Devices

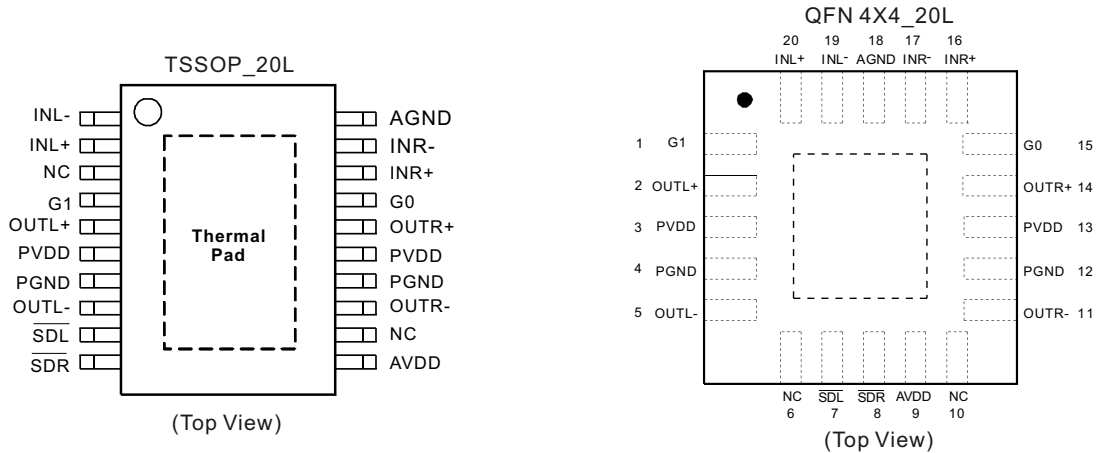
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Function Block Diagram



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Pin Configuration

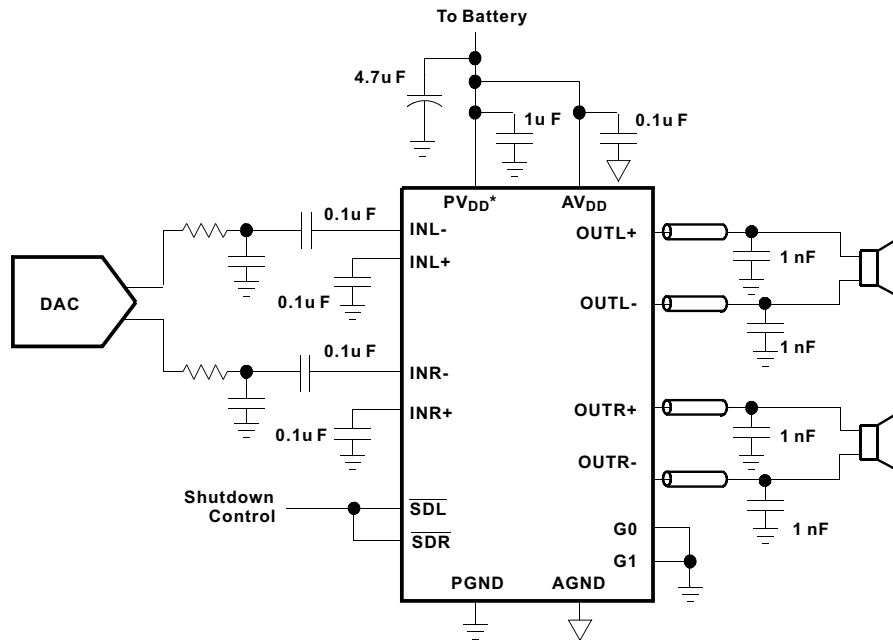


Pin Descriptions

Pin #			Symbol	Description
QFN	TSSOP20	WCSP		
16	18	D1	INR+	Right channel positive input
17	19	C1	INR-	Right channel negative input
20	2	A1	INL+	Left channel positive input
19	1	B1	INL-	Left channel negative input
8	10	B3	$\overline{\text{SDR}}$	Right channel shutdown terminal(active low)
7	9	B4	$\overline{\text{SDL}}$	Left channel shutdown terminal(active low)
15	17	C2	G0	Gain select(LSB)
1	4	B2	G1	Gain select(MSB)
3, 13	6,15	A2	PVDD	Power supply (Must be same voltage as AVDD)
9	11	D2	AVDD	Analog supply (Must be same voltage as PVDD)
4, 12	7,14	C4	PGND	Power ground
18	20	C3	AGND	Analog ground
14	16	D3	OUTR+	Right channel positive differential output
11	13	D4	OUTR-	Right channel negative differential output
2	5	A3	OUTL+	Left channel positive differential output
5	8	A4	OUTL-	Left channel negative differential output
6, 10	3,12	N/A	NC	No internal connection
ThermalPad				Connect the thermalpad of QFN or PWP package to PCB GND

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Typical Application Circuit



* For QFN, an additional capacitor is recommended for the second PV_{DD} pin.

Figure 1. Typical Application Circuit

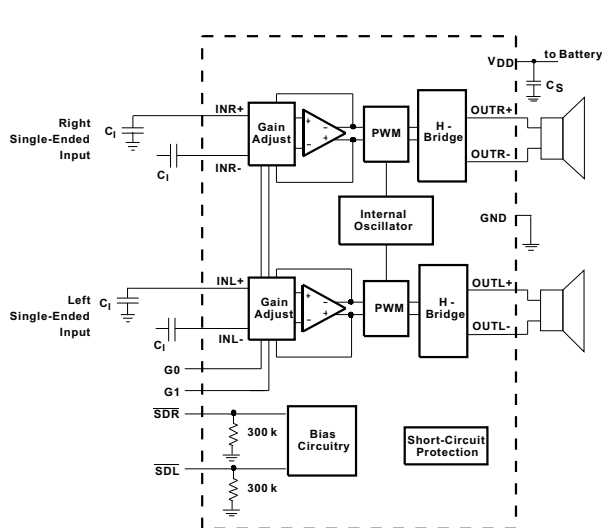


Figure 2. Application Schematic With Single-Ended Input

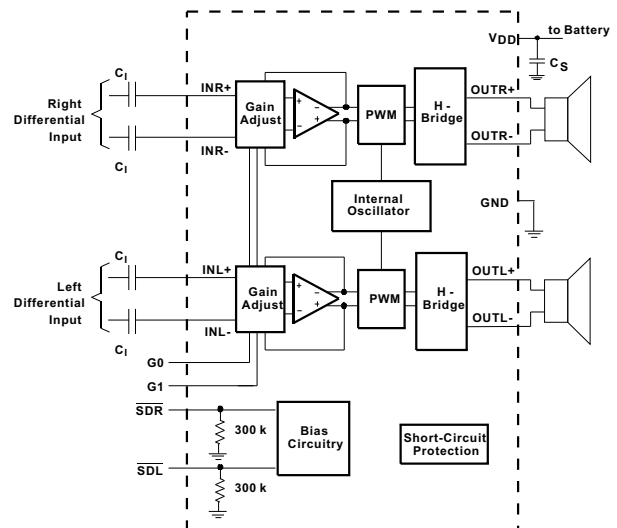


Figure 3. Application Schematic With Differential Input and Input Capacitors



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Absolute Maximum Ratings ¹

Symbol	Description	Value	Unit
V _{DD}	Supply Voltage at no Input Signal	6	V
V _I	Input Voltage	-0.3 to VDD+0.3	V
T _J	Operating Junction Temperature Range	-40 to 150	°C
T _{SDR}	Maximum Lead Soldering Temperature , 10 Seconds	260	°C
T _{STG}	Storage Temperature Range	-65 to 150	°C



Recommended Operating Conditions

Symbol	Description	Value	Unit
V _{DD}	Supply Voltage	2.5~5.5	V
T _A	Ambient Temperature Range	-40~85	°C
T _J	Junction Temperature Range	-40~125	°C

Thermal Information ²

Symbol	Description	Value	Unit
θ _{JA}	Thermal Resistance-Junction to Ambient	47	°C/W
θ _{JC}	Thermal Resistance-Junction to Case	10	°C/W

Ordering and Marking Information

Device	Package Type	Device Marking	Reel Size	Tape Width	Quantity
MD2012	QFN 4X4-20L		13"	12mm	5000 units
MD2012	TSSOP_20L		13"	12mm	3000 units

ESD Susceptibility

ESD Susceptibility-HBM ----- 2kV

ESD Susceptibility-MM ----- 200V

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at one time.
2. The ThermalPad on the bottom of the IC should be soldered directly to the PCB's ThermalPad area that has several thermal vias connect to the ground plane, and the PCB is a 2-layer, 5-inch square area with 2oz copper thickness.

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Electrical Characteristics

 $T_A = 25^\circ\text{C}$ (unless otherwise noted)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
$ V_{OO} $	Output offset voltage (measured differentially)	Inputs ac grounded, $A_V=6\text{dB}$, $V_{DD}=2.7\text{V to }5.5\text{V}$		5	25	mV
PSRR	Power supply rejection ratio	$V_{DD}=2.7\text{V to }5.5\text{V}$		-75	-55	dB
CMRR	Common mode rejection ratio	Inputs shorted together, $V_{DD}=2.7\text{V to }5.5\text{V}$		-70	-50	dB
$ I_{IH} $	High-level input current	$V_{DD}=5.5\text{V}$, $V_I=V_{DD}$			50	μA
$ I_{IL} $	Low-level input current	$V_{DD}=5.5\text{V}$, $V_I=0\text{V}$			5	μA
I_{DD}	Supply current	$V_{DD}=5.5\text{V}$, no load or output filter		7.5		mA
		$V_{DD}=3.6\text{V}$, no load or output filter		5.5		
I_{SD}	Shutdown current			0.1		μA
$r_{DS(ON)}$	Static Drain-source On-state Resistance	$V_{DD}=5.5\text{V}$		420		m Ω
		$V_{DD}=3.6\text{V}$		520		
	Output impedance in SHUTDOWN	$V_{(SHUTDOWN)}=0.35\text{V}$		2		k Ω
$f_{(SW)}$	Switching frequency	$V_{DD}=2.7\text{V to }5.5\text{V}$		300		KHZ
	Closed-loop voltage gain	$G_0, G_1=0.35\text{V}$		6		dB
		$G_0=V_{DD}, G_1=0.35\text{V}$		12		
		$G_0=0.35\text{V}, G_1=V_{DD}$		18		
		$G_0, G_1=V_{DD}$		24		

Operating Characteristics

 $T_A=25^\circ\text{C}$, $R_L=8\Omega$

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
P_O	Output power (per channel)	THD+N=10%, $f=1\text{kHz}$, $R_L=4\Omega$, $V_{DD}=5\text{V}$		2.7		W
		THD+N=10%, $f=1\text{kHz}$, $R_L=8\Omega$, $V_{DD}=5\text{V}$		1.5		
		$V_{DD}=3.6\text{V}$		0.75		
THD+N	Total harmonic distortion plus noise	$V_{DD}=5\text{V}$, $P_O=1\text{W}$, $A_V=6\text{dB}$, $f=1\text{kHz}$, $R_C=8\Omega$		0.14%		
		$V_{DD}=5\text{V}$, $P_O=0.5\text{W}$, $A_V=6\text{dB}$, $f=1\text{kHz}$, $R_C=8\Omega$		0.10%		
	Channel crosstalk	$V_{DD}=3.6\text{V}$, $f=1\text{KHz}$		-85		dB
k_{SVR}	Supply ripple rejection ratio	$V_{DD}=5\text{V}$, $A_V=6\text{dB}$, $f=217\text{Hz}$		-75		dB
		$V_{DD}=3.6\text{V}$, $A_V=6\text{dB}$, $f=217\text{Hz}$		-70		
V_n	Output voltage noise	$V_{DD}=3.6\text{V}$, $f=20\text{ to }20\text{KHz}$, No weighting		35		μV
		Inputs ac-grounded, $A_V=6\text{dB}$, A weighting		27		
CMRR	Common mode rejection ratio	$V_{DD}=3.6\text{V}$, $V_{IC}=1V_{pp}$, $f=217\text{Hz}$		-70		dB
Z_i	Input impedance	$A_V=6\text{dB}$		28.1		k Ω
		$A_V=12\text{dB}$		17.3		
		$A_V=18\text{dB}$		9.8		
		$A_V=24\text{dB}$		5.2		
	Start-up time from shutdown	$V_{DD}=3.6\text{V}$		3.5		ms

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Typical Performance Characteristics

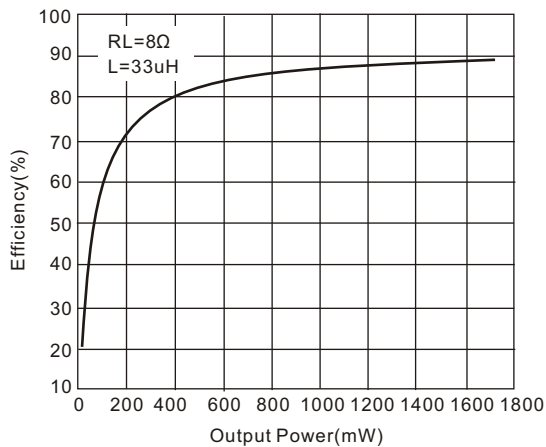


Figure 4. Efficiency vs Output Power

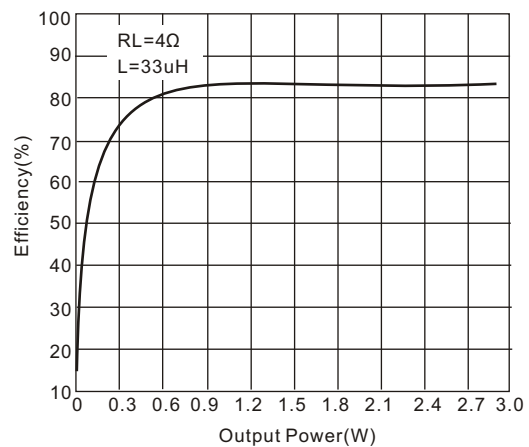


Figure 5. Efficiency vs Output Power

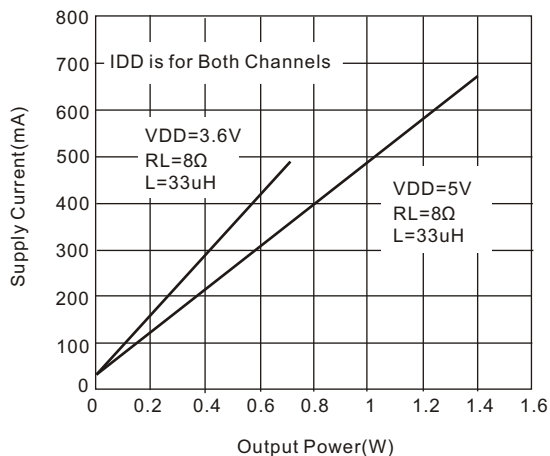


Figure 6. Supply Current vs Output Power

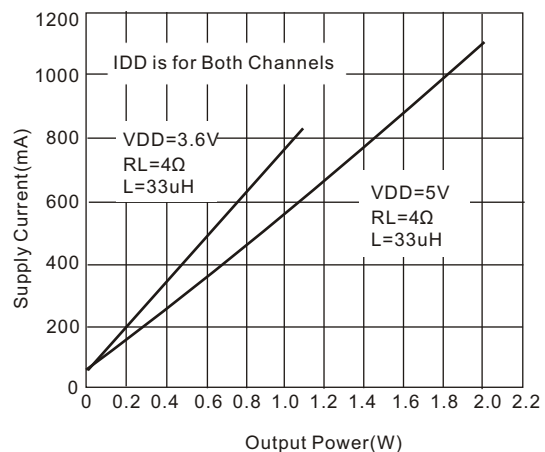


Figure 7. Supply Current vs Output Power

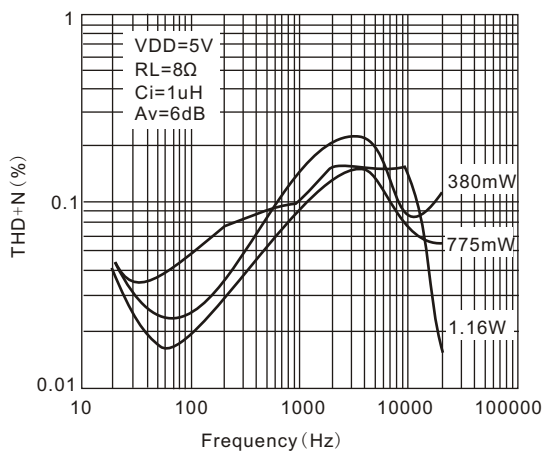


Figure 8. THD+N vs Frequency

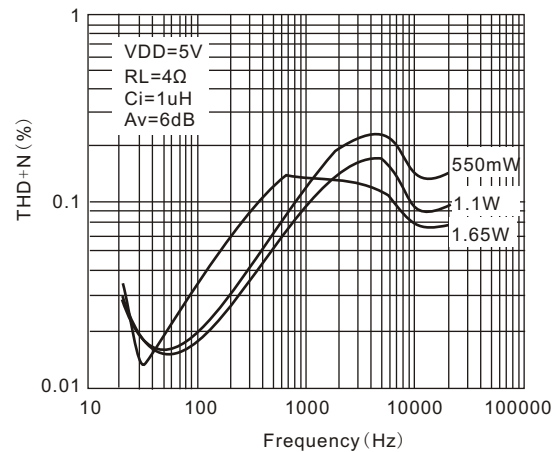


Figure 9. THD+N vs Frequency

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Typical Performance Characteristics

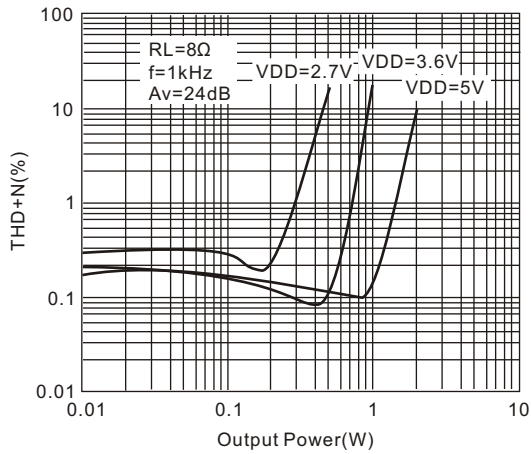


Figure 10. THD+N vs Output Power

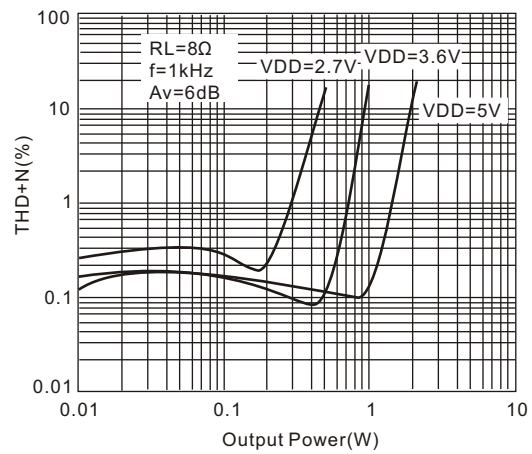


Figure 11. THD+N vs Output Power

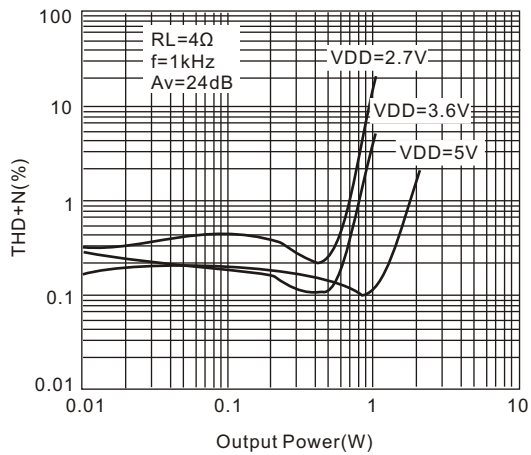


Figure 12. THD+N vs Output Power

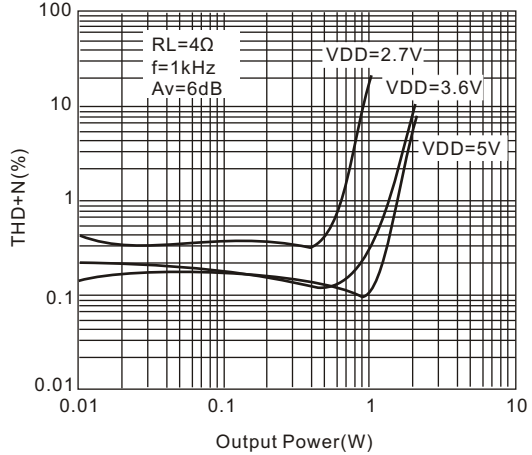


Figure 13. THD+N vs Output Power

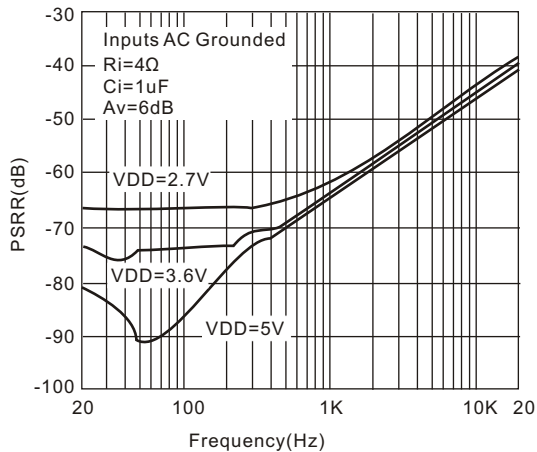


Figure 14. PSRR vs Frequency

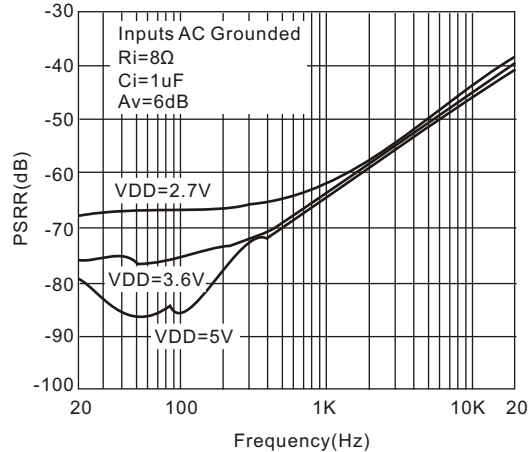


Figure 15. PSRR vs Frequency

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Typical Performance Characteristics

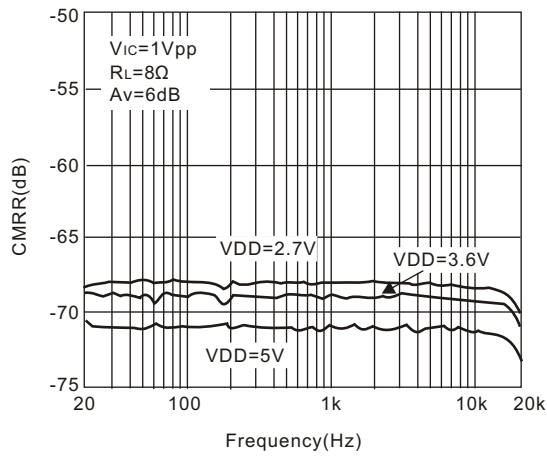


Figure 16. CMRR vs Frequency

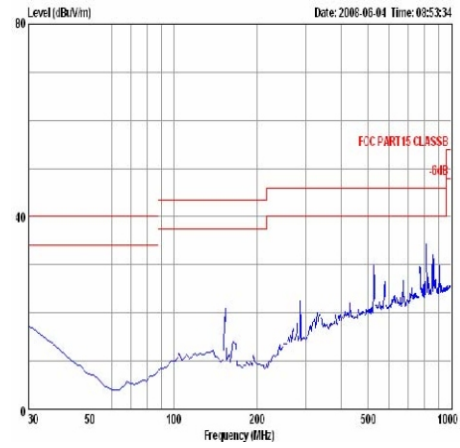


Figure 17. FCC Level



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Application Information

Decoupling Capacitor (Cs)

The MD2012 is a high-performance Class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 mF, placed as close as possible to the device PVDD lead works best. Placing this decoupling capacitor close to the MD2012 is important for the efficiency of the Class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 4.7 uF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

Table 1 Gain Setting

G1	G0	Gain (V/V)	Gain (dB)	Input Impedance (R1)(kΩ)
0	0	2	6	28.1
0	1	4	12	17.3
1	0	8	18	9.8
1	1	16	24	5.2

Input Capacitors (Ci)

The MD2012 does not require input coupling capacitors if the design uses a differential source that is biased from 0.5 V to VDD – 0.8 V. If the input signal is not biased within the recommended common-mode input range, if high pass filtering is needed (see Figure 3), or if using a single-ended source (see Figure 2), input coupling capacitors are required.

The input capacitors and input resistors form a high-pass filter with the corner frequency, f_c , determined in Equation 1.

$$f_c = \frac{1}{(2\pi R_i C_i)} \quad (1)$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application. Not using input capacitors can increase output offset.

Equation 2 is used to solve for the input coupling capacitance.

$$C_i = \frac{1}{(2\pi R_i f_c)} \quad (2)$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of $\pm 10\%$ or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

Component Location

Place all the external components very close to the MD2012. Placing the decoupling capacitor, C_s , close to the MD2012 is important for the efficiency of the Class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

Trace Width

Recommended trace width at the solder balls is 75 mm to 100 mm to prevent solder wicking onto wider PCB traces.

For high current pins (PVDD, PGND, and audio output pins) of the MD2012, use 100-mm trace widths at the solder balls and at least 500-mm PCB traces to ensure proper performance and output power for the device.

For the remaining signals of the MD2012, use 75-mm to 100-mm trace widths at the solder balls. The audio input pins (INR+/- and INL+/-) must run side-by-side to maximize common-mode noise cancellation.

Efficiency and Thermal Information

The maximum ambient temperature depends on the heat-sinking ability of the PCB system. The derating factor for the packages are shown in the dissipation rating table. Converting this to θ_{JA} for the QFN package:

$$\theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.041} = 24^\circ\text{C/W} \quad (3)$$

Given of 24°C/W , the maximum allowable junction temperature of 150°C , and the maximum internal dissipation of 1.5W (0.75 W per channel) for 2.1 W per channel, 4-Ω load, 5-V supply, the maximum ambient temperature can be calculated with the following equation.

$$T_{A\text{Max}} = T_{J\text{Max}} - \theta_{JA} P_{D\text{Max}} = 150 - 24(1.5) = 114^\circ\text{C} \quad (4)$$



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Equation 4 shows that the calculated maximum ambient temperature is 114°C at maximum power dissipation with a 5-V supply and 4-Ω a load. The MD2012 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Also, using speakers more resistive than 4-Ω dramatically increases the thermal performance by reducing the output current and increasing the efficiency of the amplifier.

Operation with DACs and CODECs

In using Class-D amplifiers with CODECs and DACs, sometimes there is an increase in the output noise floor from the audio amplifier. This occurs when mixing of the output frequencies of the CODEC/DAC mix with the switching frequencies of the audio amplifier input stage. The noise increase can be solved by placing a low-pass filter between the CODEC/DAC and audio amplifier. This filters off the high frequencies that cause the problem and allow proper performance. See Figure 1 for the block diagram.

Filter free Operation and ferrite bead filters

A ferrite bead filter can often be used if the design is failing radiated emissions without an LC filter and the frequency sensitive circuit is greater than 1 MHz. This filter functions well for circuits that just have to pass FCC and CE because FCC and CE only test radiated

emissions greater than 30 MHz. When choosing a ferrite bead, choose one with high impedance at high frequencies, and very low impedance at low frequencies. In addition, select a ferrite bead with adequate current rating to prevent distortion of the output signal.

Use an LC output filter if there are low frequency (< 1 MHz) EMI sensitive circuits and/or there are long leads from amplifier to speaker.

Figure 18 shows typical ferrite bead and LC output filters.

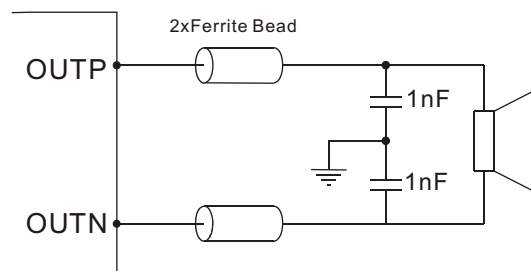
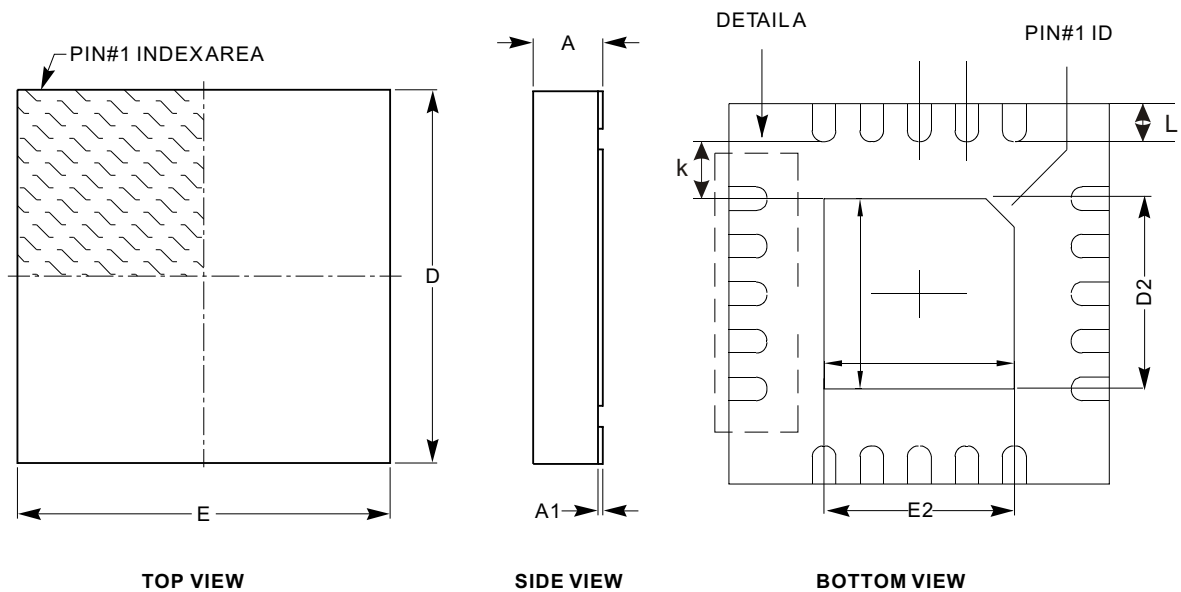


Figure 18. Typical Ferrite Chip Bead Filter

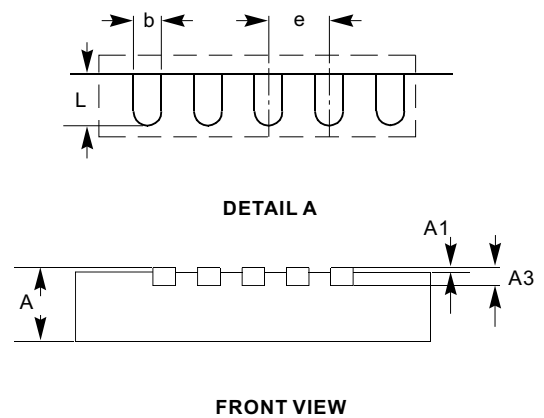
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Package Information

QFN 4X4_20L



SYMBOL	MIN	NOM	MAX
A	0.70	0.80	0.90
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.18	0.24	0.30
D	3.90	4.00	4.10
D2	1.90	-	2.10
E	3.90	4.00	4.10
E2	1.90	-	2.10
e	0.50 TYP		
L	0.30	-	0.50
k	0.20 MIN		



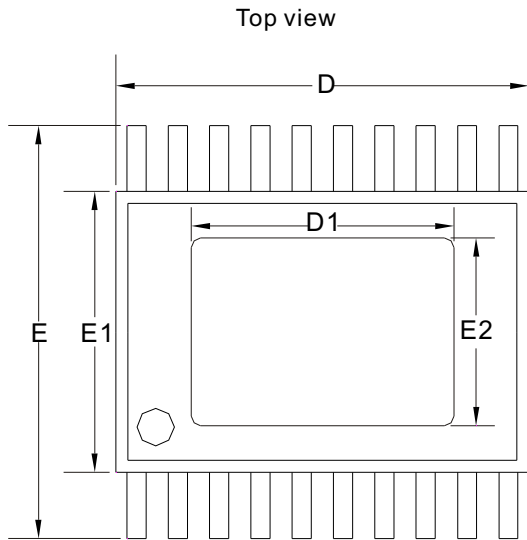
Notes:

- (1) All dimensions are in millimeters.
- (2) Refer to JEDEC standard MO-220.

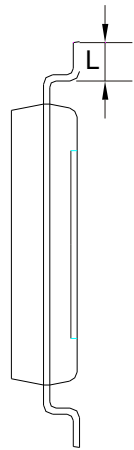
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Package Information

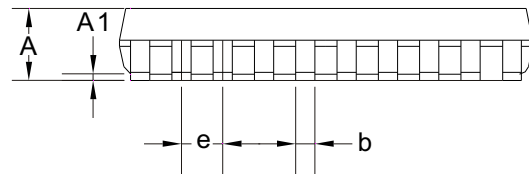
TSSOP_20L



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
	-	1.2	-	0.047
A1	0	0.15	0	0.006
b	0.19	0.3	0.007	0.012
E1	4.40		0.173	
D	6.50		0.256	
D1	3.77		0.148	
E	6.20	6.6	0.244	0.26
E2	2.70		0.106	
e	0.65		0.026	
L	0.45	0.75	0.018	0.03



End View



Side View